Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction; and

responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present; and

prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

2. (Original) The method of claim 1, wherein the prefetch indicator contains the pointer to the data structure.

3. (Canceled)

4. (Previously Presented) The method of claim 1, wherein the selectively prefetching step further includes:

determining whether to replace cache lines; and

prefetching the data in response to a determination that a number of cache lines chosen to be replaced is greater than a threshold.

5. (Currently Amended) The method of claim 1, wherein the processor unit is selected from one of an instruction cache, data cache, [[or]] and a load/store unit.

6. (Original) The method of claim 1, wherein the cache is an instruction cache.

7. (Original) The method of claim 1, wherein the cache is a data cache.

8-10. (Canceled)

11. (Previously Presented) A data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the data processing system comprising:

determining means, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction; and

selectively prefetching means, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the selectively prefetching means includes:

means for determining whether outstanding cache misses are present; and

means for prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

12. (Original) The data processing system of claim 11, wherein the prefetch indicator contains the pointer to the data structure.

13. (Canceled)

14. (Previously Presented) The data processing system of claim 11, wherein the selectively prefetching means further includes:

means for determining whether to replace cache lines; and

means for prefetching the data in response to a determination that a number of cache lines chosen to be replaced is greater than a threshold.

15. (Currently Amended) The data processing system of claim 11, wherein the processor unit is selected from one of an instruction cache, a data cache, [[or]] and a load/store unit.

16. (Original) The data processing system of claim 11, wherein the cache is an instruction cache.

17. (Original) The data processing system of claim 11, wherein the cache is a data cache.

18. (Previously Presented) A computer program product in a recordable-type computer readable medium for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the computer program product comprising:

first instructions, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction; and

second instructions, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the second instructions includes:

first sub-instructions for determining whether outstanding cache misses are present; and

second sub-instructions for prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

19. (Original) The computer program product of claim 18, wherein the prefetch indicator contains the pointer to the data structure.

20. (Canceled)

21. (Previously Presented) The computer program product of claim 18, wherein the second instructions further includes:

first sub-instructions for determining whether to replace cache lines; and

second sub-instructions for prefetching the data in response to a determination that a number of cache lines chosen to be replaced is greater than a threshold.

22. (Currently Amended) The computer program product of claim 18, wherein the processor unit is selected from one of an instruction cache, a data cache, [[or]] and a load/store unit.

23. (Original) The computer program product of claim 18, wherein the cache is an instruction cache.

24. (Original) The computer program product of claim 18, wherein the cache is a data cache.

25. (Previously Presented) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction, wherein the processor unit is selected from one of an instruction cache, a data cache, and a load/store unit; and

responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the selectively prefetching step includes:

determining that outstanding cache misses are present; and

prefetching the data in response to a determination that a number of the outstanding cache misses is less than a threshold, and wherein selectively prefetching step further includes:

determining to replace cache lines; and

prefetching the data in response to a determination that a number of the cache lines chosen to be replaced is greater than a threshold.